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APPLICANT : NEC CORP;

INVENTOR : HIRANO YUICHI;

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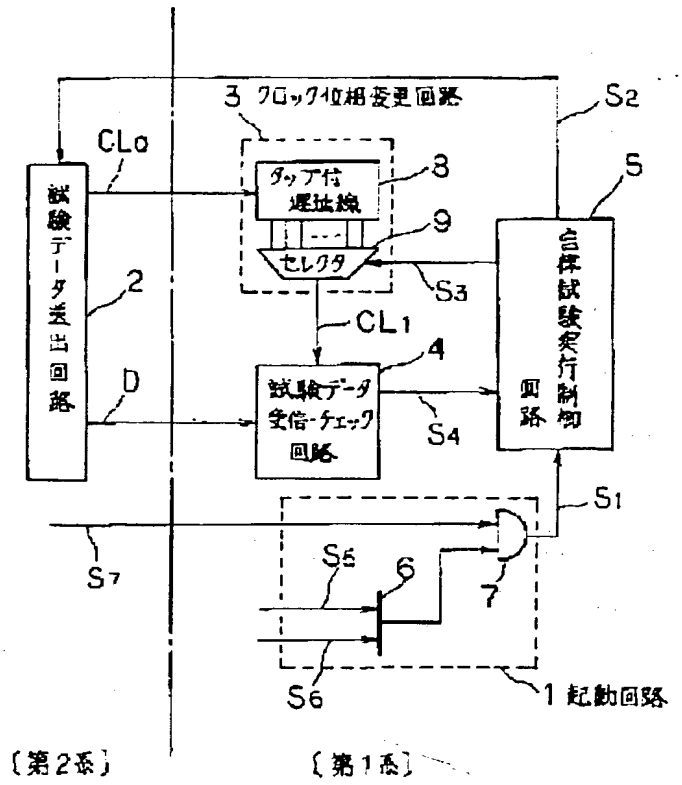
TITLE : AUTOMATIC CLOCK PHASE ADJUSTING SYSTEM AND DUPLEX DATA PROCESSOR WITH AUTOMATIC CLOCK PHASE ADJUSTING FUNCTION



ABSTRACT : PURPOSE: To dispense with a dedicated testing machine and test process expenses for phase adjustment by setting a value of clock position selection signal equivalent to an almost center point in a clock phase range as an appropriate clock phase selection signal value.

CONSTITUTION: An autonomous test execution control circuit 5 asserts a test data sending instruction signal S_2 to another system, and a test data sending circuit 2 of another system sends out test data. The data reception check circuit 4 of its own system performs the reception processing of the test data from another system synchronizing with a clock signal CL_1, and checks a data error. The autonomous test execution control circuit 5 adds one on a value of clock phase selection signal S_3 when a test result display signal S_4 displays a defective result, and changes the clock phase selected at a selector by prescribed phase difference. In such a way, the value of clock phase selection signal with satisfactory autonomous test result for data reception nearest to the center of the clock phase range is set as the clock phase selection signal S_3.